What is claimed is:

1. A method of forming a dual damascene structure for copper dual damascene processes, comprising the steps of:

providing a substrate, said substrate having been provided with semiconductor devices structures in or on the surface thereof, at least one point of electrical contact having been provided in the surface of said substrate, a layer of Inter Metal Dielectric (IMD) having been deposited over the surface of said substrate, at least one opening having been created through said layer of IMD, said at least one opening being aligned with said at least one point of electrical contact having been provided in the surface of said substrate;

depositing a layer of first semiconductor material over the surface of said layer of IMD, filling said at least one opening created through said layer of IMD;

removing said layer of first semiconductor material from the surface of said layer of IMD, thereby partially removing said first semiconductor material from said at least one opening created through said layer of IMD, creating at least one partial opening through said layer of IMD;

baking said substrate for a period of time by applying an elevated temperature in a gaseous environment and under a pressure to said substrate;

depositing a layer of second semiconductor material over the surface of said layer of IMD, thereby filling said at least one partial opening created through said layer of IMD; and

patterning and etching said layer of second semiconductor material, creating an opening through said layer of second semiconductor material that aligns with said at least one partial opening created through said layer of IMD, removing said layer of second semiconductor material from said at least one partial opening created through said layer of IMD.

2. The method of claim 1, said first semiconductor material comprising I-line photoresist.

3. The method of claim 1, said second semiconductor material comprising DUV photoresist.

4. The method of claim 1, wherein said baking said substrate comprises baking said substrate on a hot plate.

5. The method of claim 1, wherein said baking said substrate comprises baking said substrate inside a high-temperature furnace.

6. The method of claim 1, wherein said applying an elevated temperature comprises applying a temperature between about 200 and 400 degrees C.

7. The method of claim 1, wherein said pressure comprises a low pressure environment of between about 40 and 60 pa.

8. The method of claim 1, wherein said pressure comprises an atmospheric pressure.

9. The method of claim 1, wherein said gaseous environment may or may not contain an inert gas.

10. The method of claim 1, wherein said gaseous environment may or may not contain an annealing agent that is typically applied for an anneal environment in which a metal is present.

11. The method of claim 10, wherein said annealing agent is selected from the group consisting of H_2 and N_2 and NH_3.

12. The method of claim 1, wherein said period of time is between about 1 and 30 minutes.

13. The method of claim 1, with additional steps being performed after said patterning and etching said second layer of semiconductor material, said additional steps comprising:

depositing a layer of copper over the surface of said second layer of semiconductor material, thereby filling said opening created through said second layer of semiconductor material that aligns with said at least one partial opening created through said layer of IMD, thereby further filling said at least one partial opening created through said layer of IMD; and

removing said deposited layer of copper from the surface of said layer of second semiconductor material.

14. The method of claim 13, said step of removing said deposited layer of copper from the surface of said layer of second semiconductor material comprising steps of copper etch.

15. The method of claim 13, said step of removing said deposited layer of copper from the surface of said layer of second semiconductor material comprising steps of Chemical Mechanical Polishing (CMP).

16. The method of claim 1, said layer of IMD comprising a layer of low-k dielectric.

17. The method of claim 1, said at least one opening having been created through said layer of IMD comprising applying a wet etch process.

18. A method of forming a dual damascene structure for copper dual damascene processes, comprising the steps of:

providing a substrate, said substrate having been provided with semiconductor devices structures in or on the surface thereof, at least one point of electrical contact having been provided in the surface of said substrate;

depositing a first layer of dielectric over the surface of said substrate;

creating at least one first opening through said first layer of dielectric, said at least one first opening being aligned with said at least one point of electrical contact having been provided in the surface of said substrate;

creating a layer of protective material over a bottom surface of said at least one first opening;

baking said substrate, including said first layer of dielectric and said layer of protective material over a bottom surface of said at least one first opening;

depositing a second layer of dielectric over the surface of said first layer of dielectric, filling said at least one first opening;

creating at least one second opening through said second layer of dielectric, said at least one second opening being aligned with said at least one first opening.

19. The method of claim 18, said creating a layer of protective material over a bottom surface of said at least one first opening comprising the steps of:

depositing a layer of protective material over the surface of said first layer of dielectric, filling said at least one opening created through said first layer of dielectric;

removing said layer of protective material from the surface of said first layer of dielectric, thereby partially removing said protective material from said at least one opening created through said first layer of dielectric, creating at least one partial opening through said first layer of dielectric.

20. The method of claim 19, said protective material comprising I-line photoresist.

21. The method of claim 18, said first layer of dielectric comprising Inter Metal Dielectric (IMD).

22. The method of claim 18, said second layer of dielectric comprising DUV photoresist.

23. The method of claim 18, said baking said substrate, including said first layer of dielectric and said layer of protective material over a bottom surface of said at least one first opening comprising baking said substrate for a period of time by applying an elevated temperature in a gaseous environment and under a pressure to said substrate.

24. The method of claim 23, wherein said baking said substrate comprises baking said substrate on a hot plate.

25. The method of claim 23, wherein said baking said substrate comprises baking said substrate inside a high-temperature furnace.

26. The method of claim 23, wherein said applying an elevated temperature comprises applying a temperature between about 200 and 400 degrees C.

27. The method of claim 23, wherein said pressure comprises a low pressure environment of between about 40 and 60 pa.

28. The method of claim 23, wherein said pressure comprises an atmospheric pressure.

29. The method of claim 23, wherein said gaseous environment may or may not contain an inert gas.

30. The method of claim 23, wherein said gaseous environment may or may not contain an annealing agent that is typically applied for an anneal environment in which a metal is present.

31. The method of claim 30, wherein said annealing agent is selected from the group consisting of H_2 and N_2 and NH_3.

32. The method of claim 23, wherein said period of time is between about 1 and 30 minutes.

33. The method of claim 18, with additional steps being performed after creating at least one second opening through said second layer of dielectric, said additional steps comprising:

depositing a layer of copper over the surface of said second layer of dielectric, thereby filling said at least one opening created through said second layer of dielectric that aligns with said at least one partial opening created through said first layer of dielectric, thereby further filling said at least one partial opening created through said first layer of dielectric; and

removing said deposited layer of copper from the surface of said second layer of dielectric.

34. The method of claim 33, said step of removing said deposited layer of copper from the surface of said second layer of dielectric comprising steps of copper etch.

35. The method of claim 33, said step of removing said deposited layer of copper from the surface of said second layer of dielectric comprising steps of Chemical Mechanical Polishing (CMP).

36. The method of claim 18, said first layer of dielectric comprising a layer of low-k dielectric.

37. The method of claim 18, said at least one opening having been created through said first layer of dielectric comprising applying a wet etch process.